VLSI Design and Simulation

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Area estimation

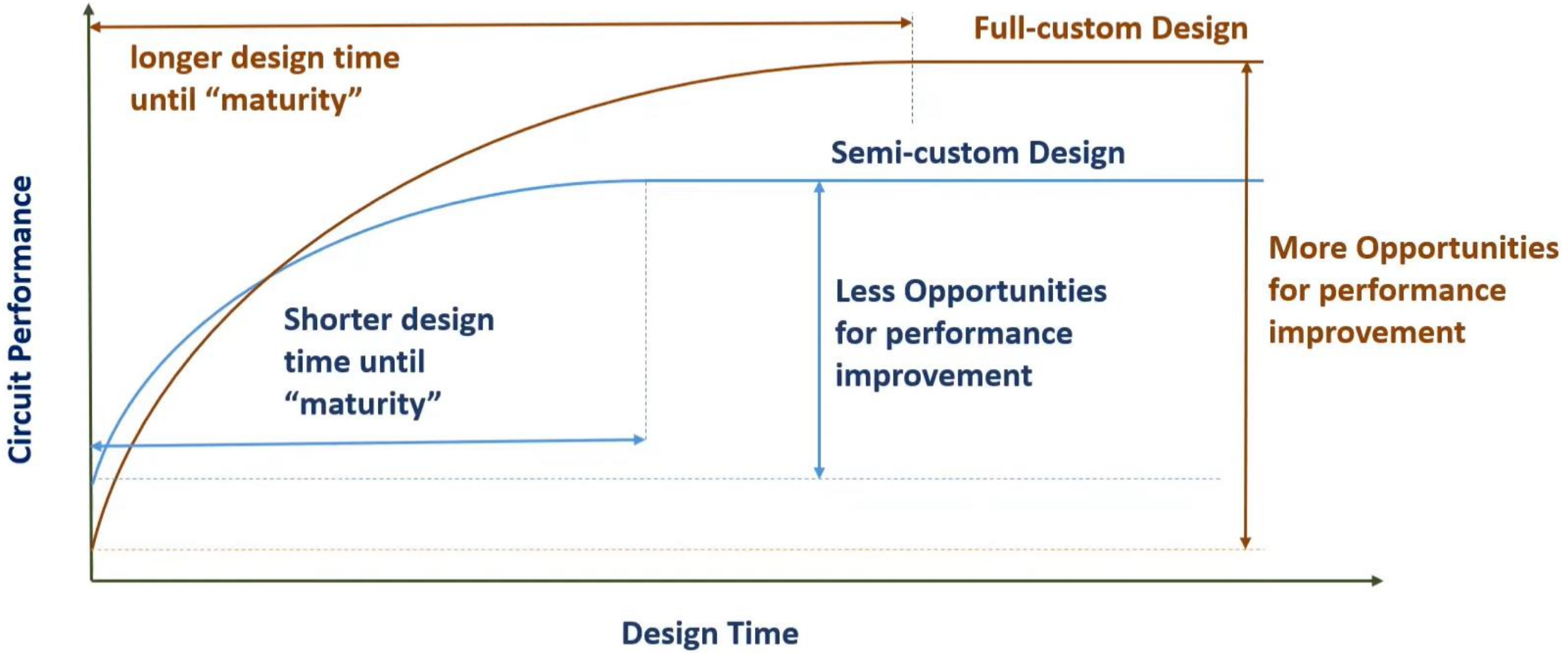
Semi Custom VLSI Design

1. Some commonly used design, layout, geometry and placement of transistor is interfaced with given demand.
2. Design is completed with the use of multiple library.
3. Development time for design before maturity is less.
4. It has less opportunity for performance improvement
5. Complete dependency on existing technology.
6. Low cost

Full Custom VLSI Design

1. Complete design, layout, geometry, orientation and placement of transistor is done by designer
2. Entire design is made without use of any library.
3. Development time for design before maturity is more.
4. It has more opportunity for performance improvement
5. Less dependency on existing technology.
6. High Cost

Performance Analysis vs. Design time



ASIC vs. FPGA

❑ ASIC Advantages:

- ➢ Faster
- ➢ Lower power
- ➢ Cheaper (if manufactured in large volumes)
- ➢ Use less transistors per logic function

❑ ASIC Drawbacks:

- ➢ Implements a particular design (not programmable)
- ➢ Takes several months to fabricate (long turn-around)
- ➢ More expensive design tools
- ➢ Very expensive engineering/mask cost for the first successful design

ASIC vs. FPGA

❑ FPGA Advantages:

- ➢ Fast programming and testing time by the end user (instant turn-around)
- ➢ Excellent for prototyping
  - ■ Easy to migrate from prototype to the final design
- ➢ Can be re-used for other designs
- ➢ Cheaper (in small volumes) ⟹ lower start-up costs
- ➢ Re-programmable
- ➢ Lower financial risk
- ➢ Ease of design changes/modifications
- ➢ Cheaper design tools

ASIC vs. FPGA

- **FPGA Drawbacks:**
  - Slower than ASIC (2-3 times slower)
  - Power hungry (up to 10 times more dynamic power)
  - Use more transistors per logic function
  - More area (20 to 35 times more area than a standard cell ASIC)

Define epitaxy, oxidation, etching, diffusion, ion implantation, metallization, photolithography.

- **Epitaxy** means a deposition or growth of a semiconductor layer upon a substrate.
- **Oxidation** is used to create a silicon dioxide (SiO2) layer on the surface of a silicon by exposing a surface to reaction with oxygen at a high temperature.

- **Etching** is used to remove a selected part of a layer.
- **Diffusion** is the movement of impurity atoms from surface into the substrate at high temperature.
- **Ion Implantation** is used for inserting impurities into a substrate.
- **Metallization** produces a metal layer on the surface, to make the interconnections between components.
- **Photolithography** is used to transfer a geometrical shape (circuit layout) from a mask to a light-sensitive material called photoresist on a substrate, by exposure to the ultraviolet (UV) light with a wavelength in the range of nanometers.

What are the main types of a photoresist?

There are two types of photoresists: positive and negative:

- In the case of the positive photoresist: the exposed areas of the positive photoresist become soft and washed away by a chemical, whereas the unexposed areas remain at the surface.
- In the case of the negative photoresist: the negative photoresist becomes hard beneath the transparent regions of the mask and the unexposed area is removed.

What are the differences between LOCOS and STI?

LOCal Oxidation of Silicon (LOCOS):

- In this method, thick oxide region (called field oxide, FOX) is created between components.
- The region without the thick oxide is known as the active area (where components are to be formed).
- The process sequence begins with growing a thin oxide layer over the Si substrate.
- Then, a silicon nitride layer is deposited over the thin oxide layer.
- After that, the silicon nitride layer and the thin oxide layer are patterned by a photolithography process.
- After this, an oxidation process is performed to create the field oxide.
- Once the field oxide has grown, the silicon nitride and the thin oxide are removed.
- The limitation to LOCOS is some lateral oxidation, leading to the bird beak shape of the field oxide, LOCOS bird beak reduces active area, thereby reducing integration density.
- The advantages of LOCOS isolation are the simple process flow and the high oxide quality because the whole LOCOS structure is thermally grown.

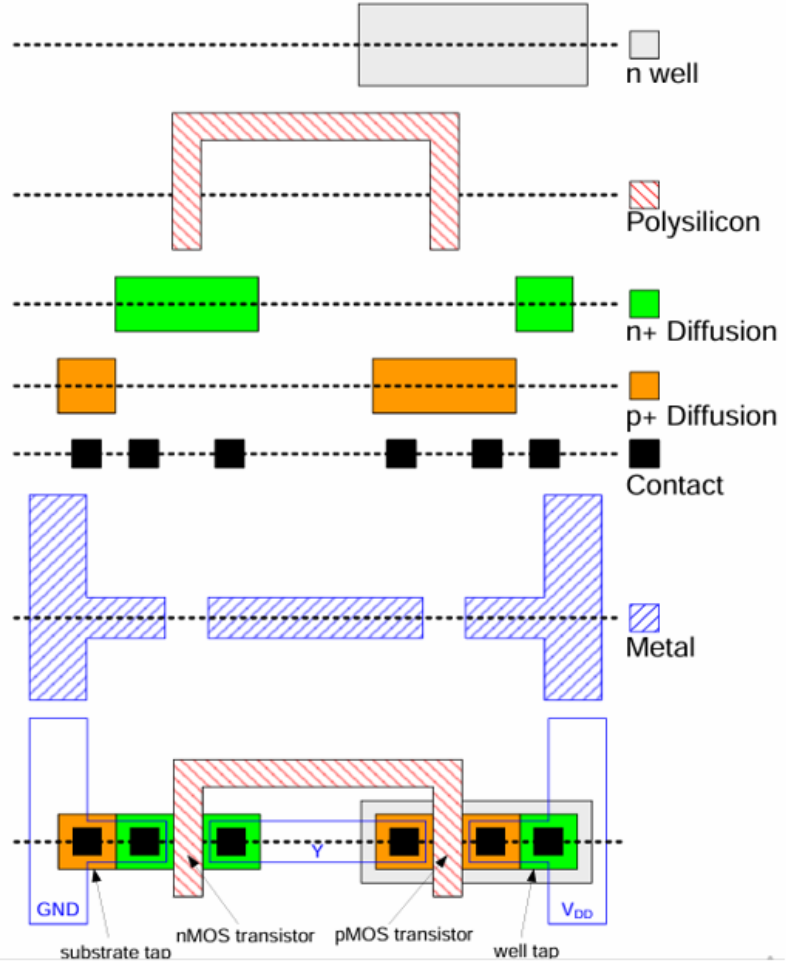
What are the differences between LOCOS and STI?

Shallow Trench Isolation (STI)

- In this method, a shallow trench is etched into the silicon substrate and then filled with the isolated oxide (FOX).
- The process sequence begins with deposition of silicon nitride over a thin oxide layer over the surface.
- Then, the silicon nitride layer and the thin oxide are patterned by a photolithography process to open windows in the areas that are to be oxidized.
- Then, an oxidation process is performed to create the isolated oxide.
- After the field oxide growth, the silicon nitride and the thin oxide are removed.
- From a processing perspective, STI is complex.
- STI is more suitable for the increased density requirements, because it allows to form smaller isolation regions with minimum lateral oxidation.

State the fabrication masks needed for CMOS inverter

- Six masks
  1. N-well
  2. Polysilicon
  3. n+ diffusion
  4. p+ diffusion
  5. Contact
  6. Metal

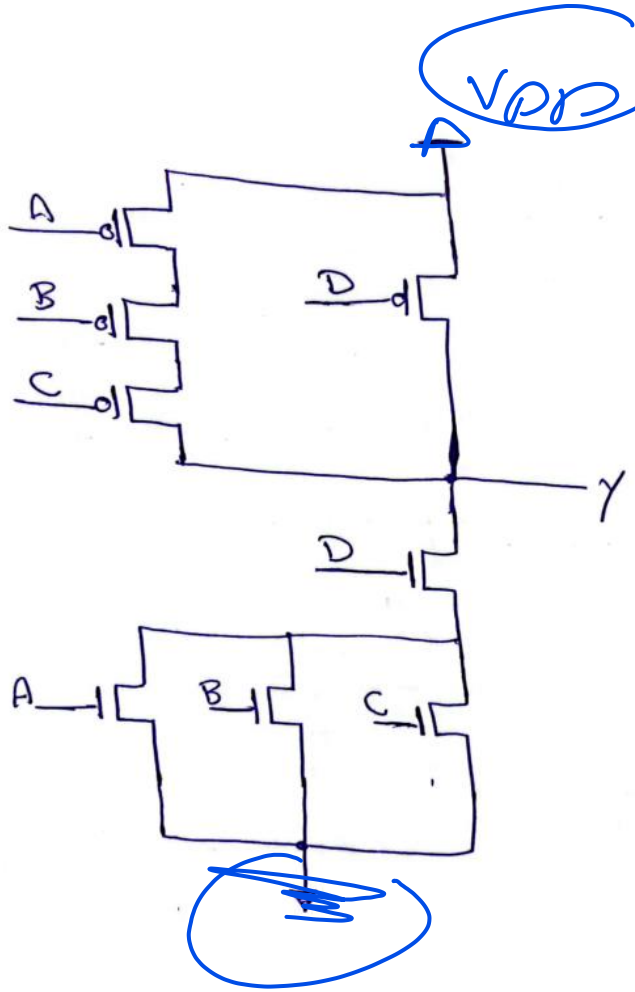


Example.1

Sketch a static CMOS gate computing

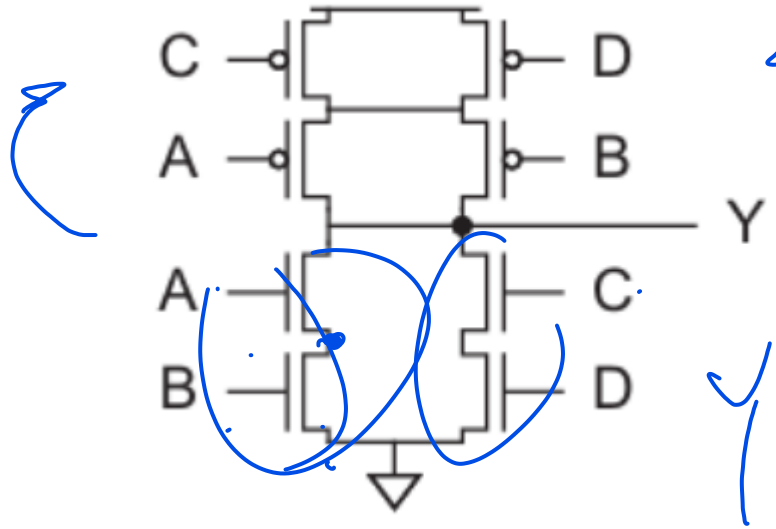
$$Y = \overline{(A + B + C) \cdot D}$$

- Solution:



Example.2

Find the logic expression for the following gate



$$Y = \overline{(A \cdot B) + (C \cdot D)}$$

- Solution:

$$Y = \overline{A \cdot B + C \cdot D}$$

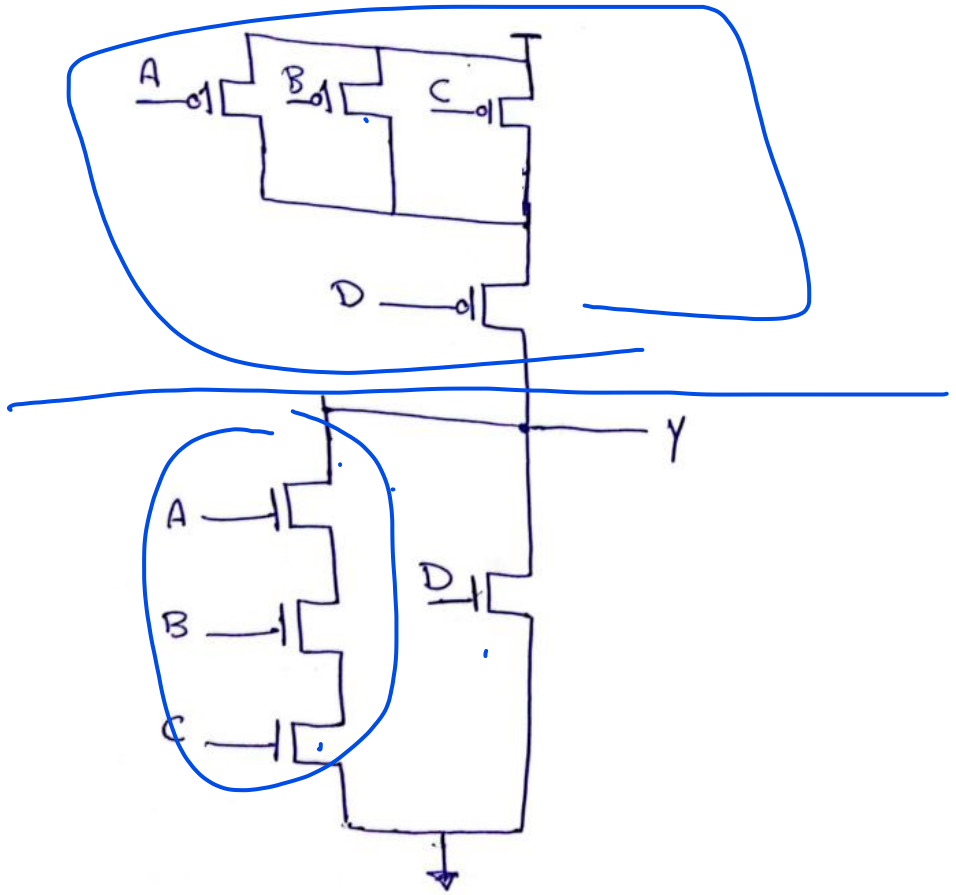
the logic expression

Example.3

Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions:

a) $Y = \overline{ABC + D}$

- Solution:

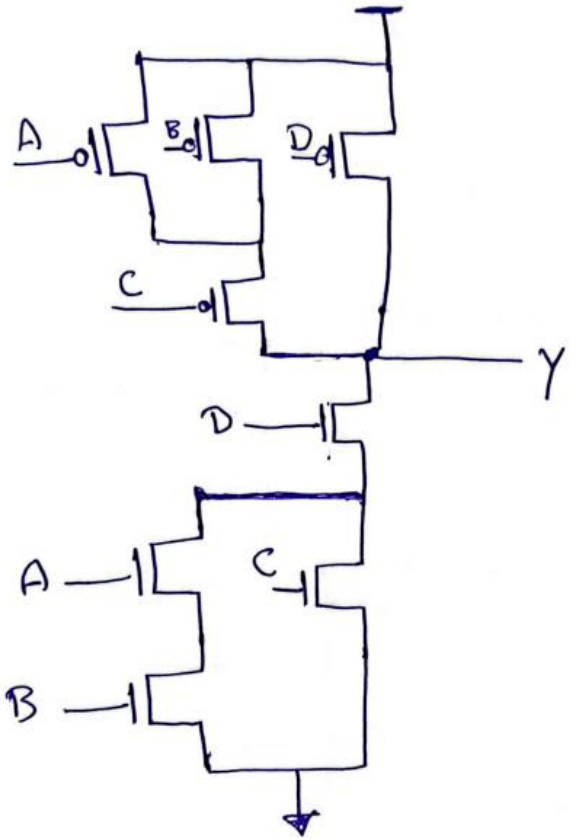


Example.4

Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions:

b) $Y = \overline{(AB + C) \cdot D}$

- Solution:

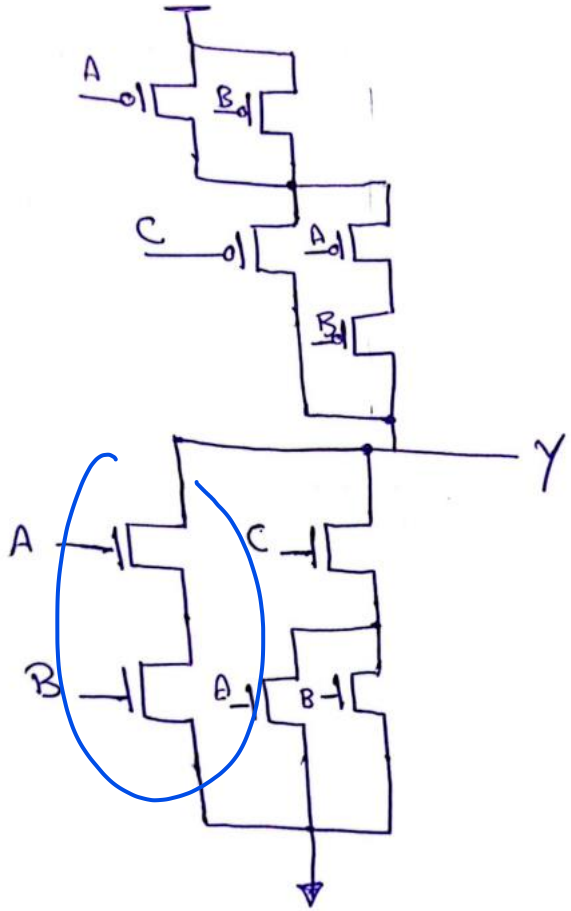


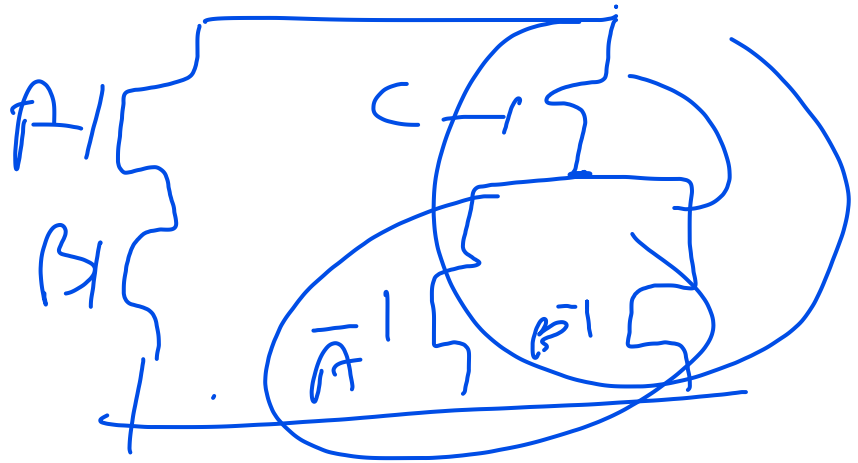
Example.5

Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions:

c) $Y = \overline{AB + C \cdot (A + B)}$

- Solution:

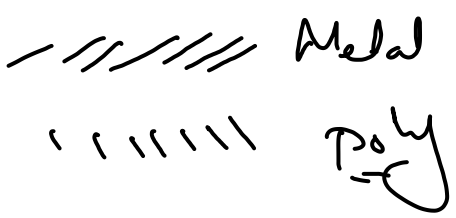


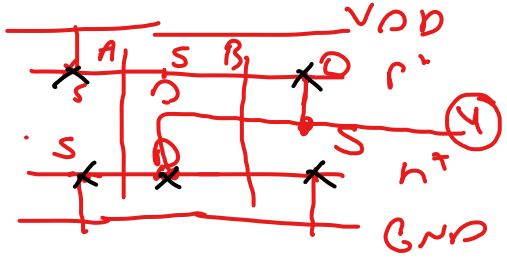


Example.6

Layout 2-input NOR gate using unit-sized transistors.

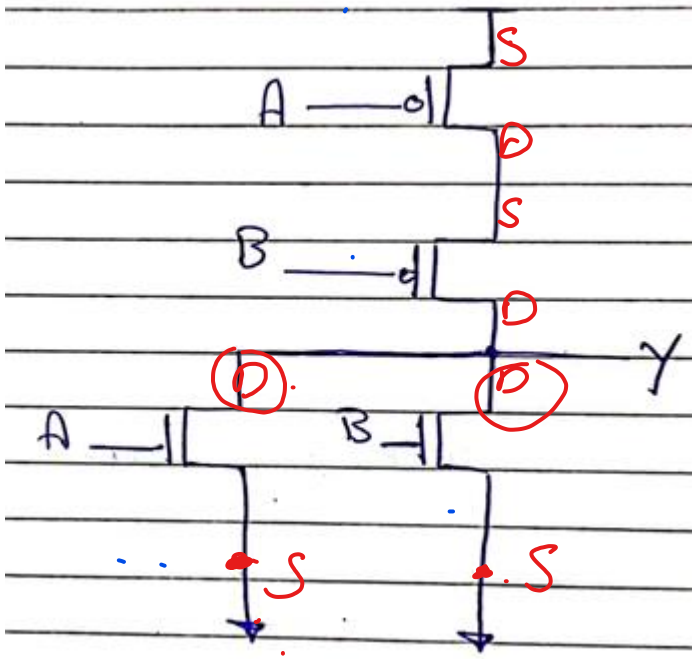
$Y = \overline{A + B}$

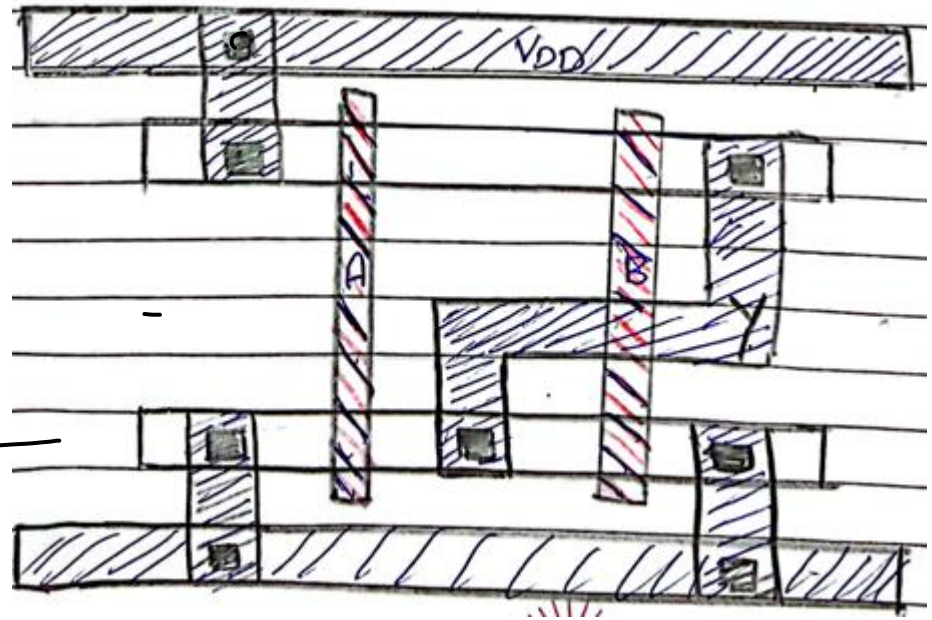




- Solution:

CMOS NOR 2-input





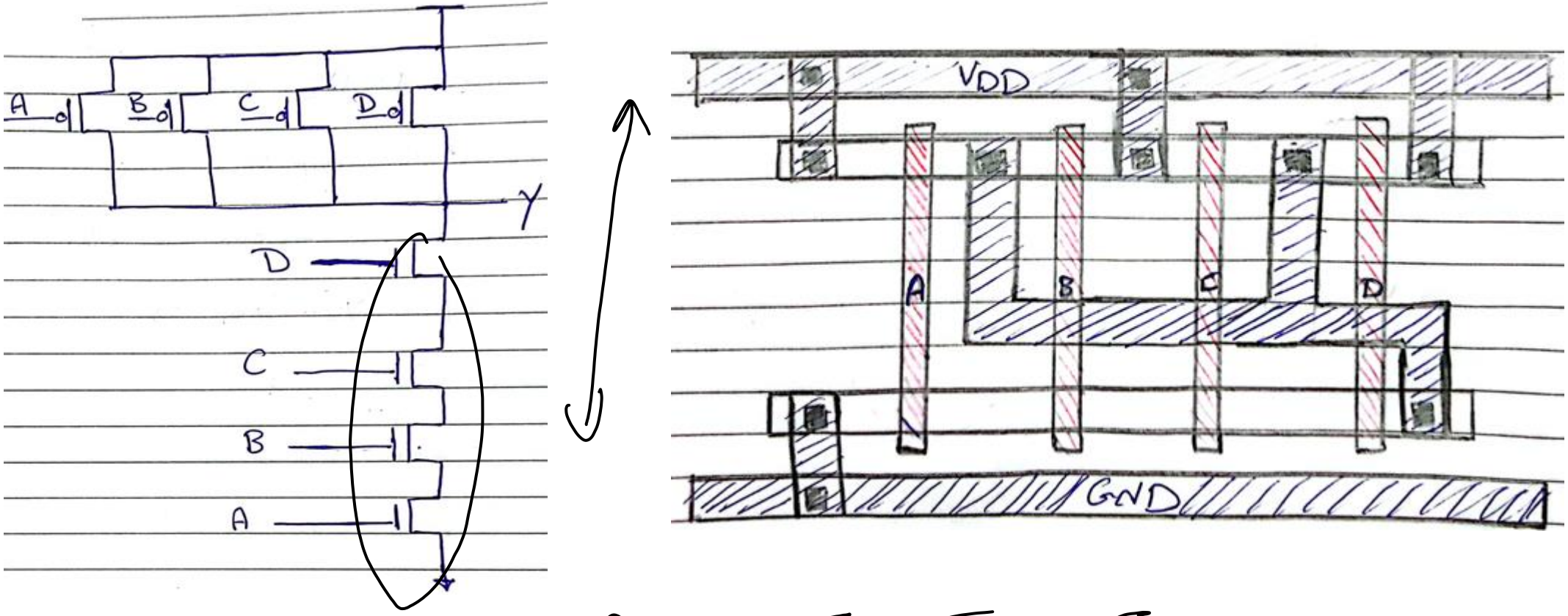
Area = hight × Width

5 WT × 3 WT = [5 × 8 λ][3 × 8 λ] λ²

Example.7

Layout 4-input NAND gate using unit-sized transistors.

$Y = \overline{A \cdot B \cdot C \cdot D}$

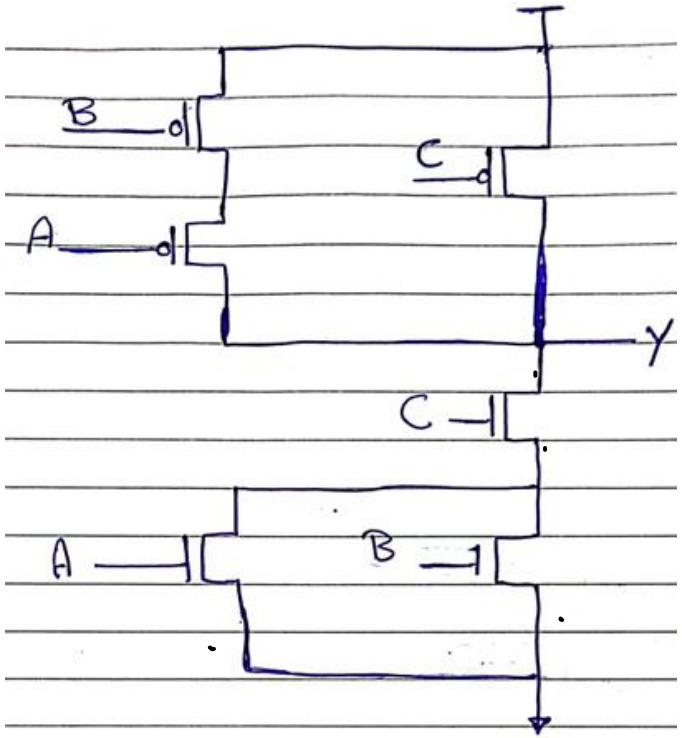


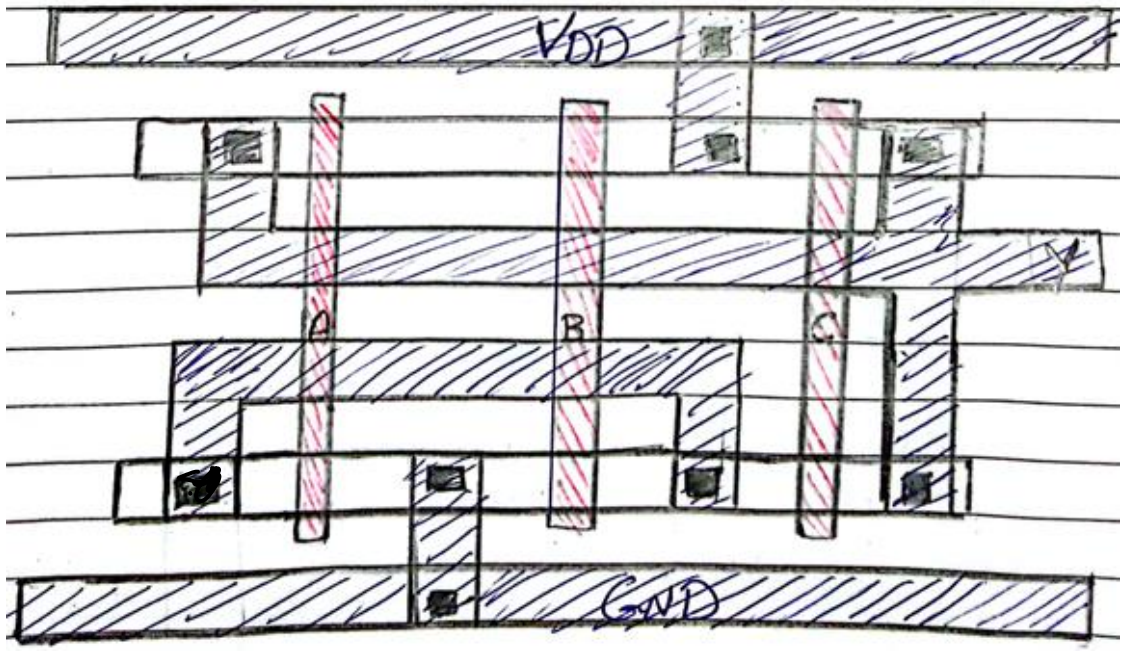
Area = 5WT ∝ 5WT

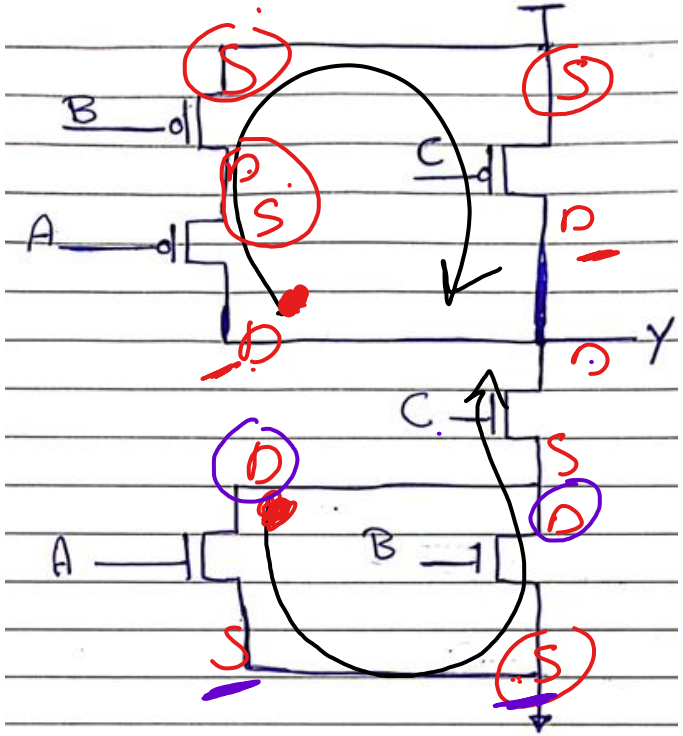
Example.8

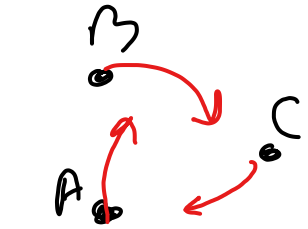
Sketch a transistor-level schematic for a CMOS gate computing $Y = \overline{(A + B).C}$ and layout your gate using unit-sized transistors.

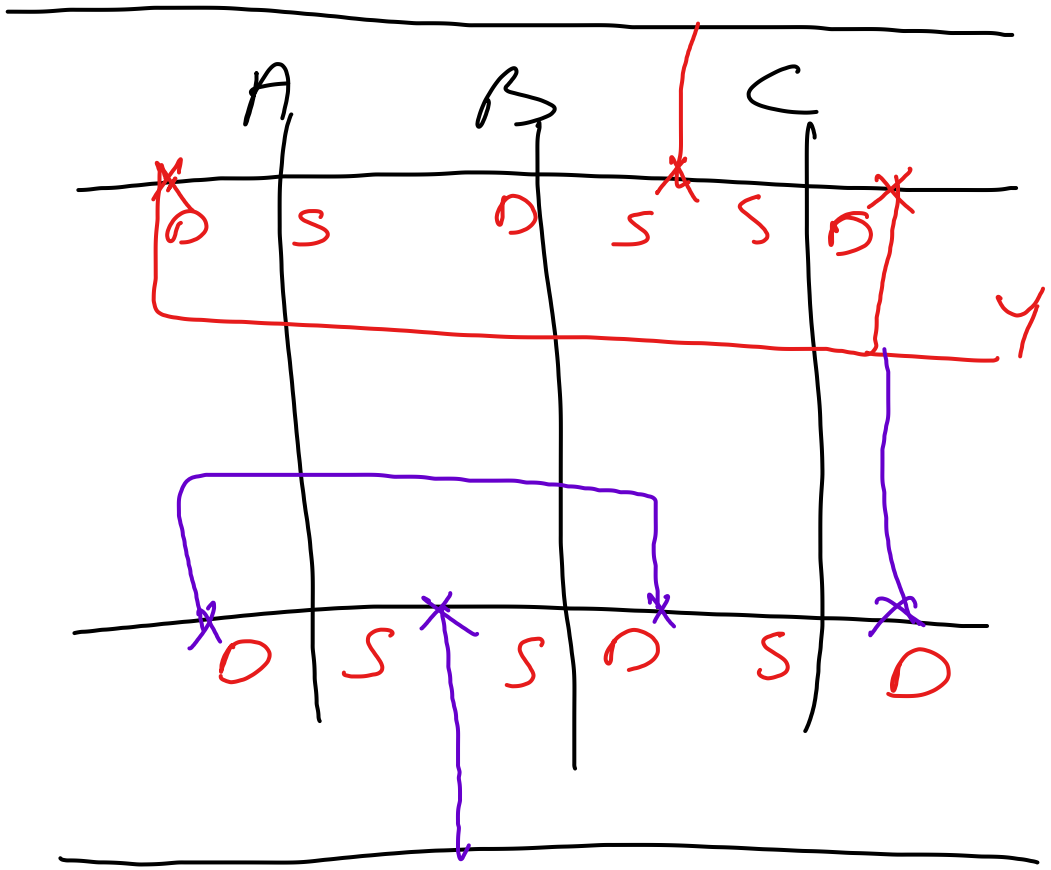
- Solution:











Stick Diagram

Example.9

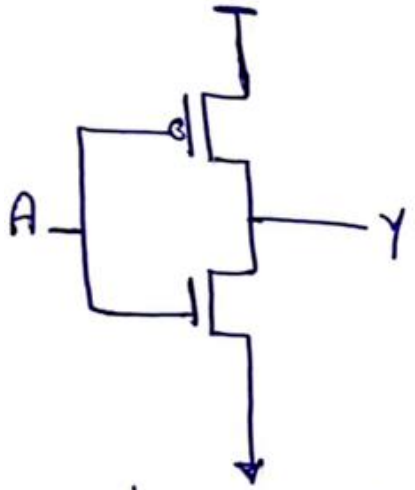
Sketch a stick diagram for the inverter CMOS gate and estimate the cell width and height using min size transistors.

- Solution:

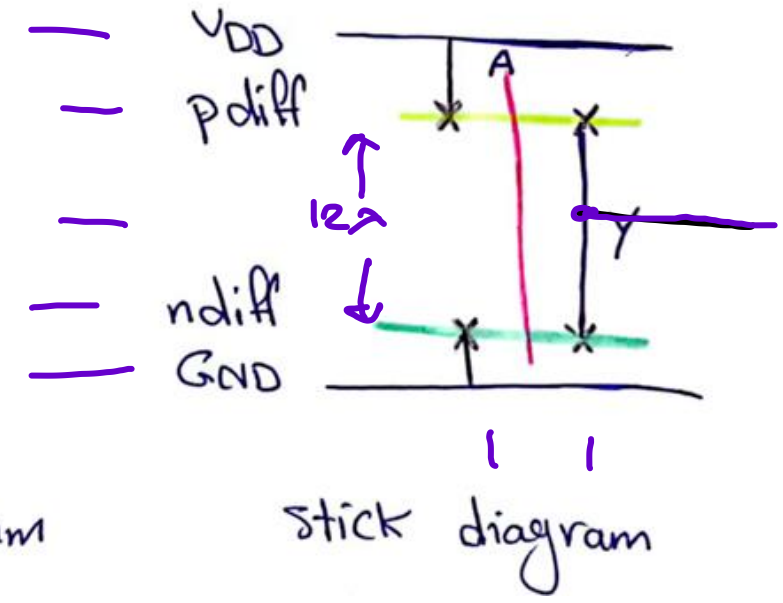
Cell height = 5WT = x8λ = λ

Cell width = 2WT = 2 x 8λ = 16λ

∴ Area = 16λ x 40λ



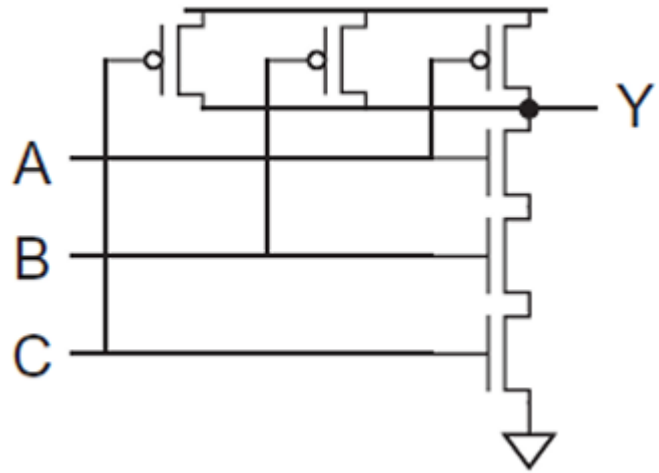
Schematic diagram



Stick diagram

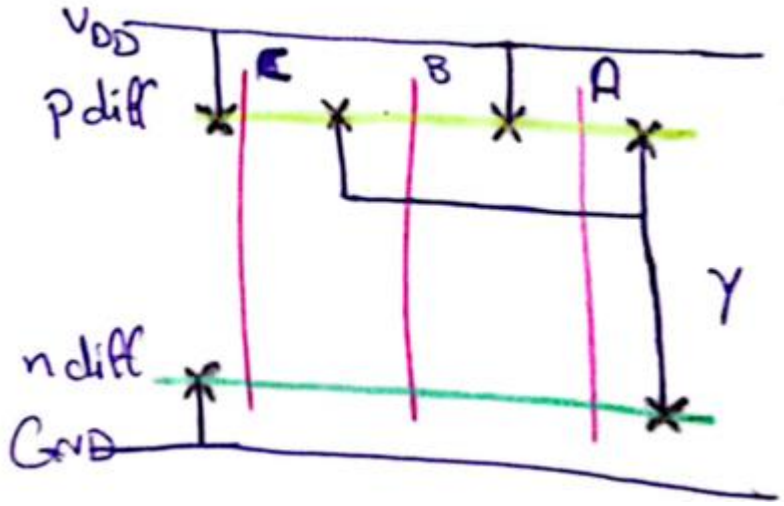
Example.10

For the shown CMOS gate find the logic expression, sketch a stick diagram and estimate the cell area using min size transistors



- Solution: $F = \overline{A.B.C}$

The stick diagram:-



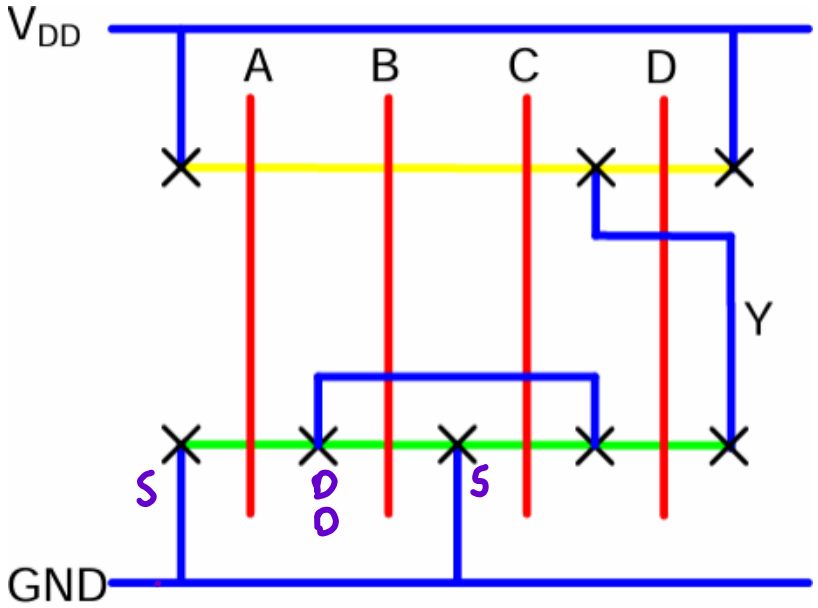
Cell height = 5 WT = 40 λ

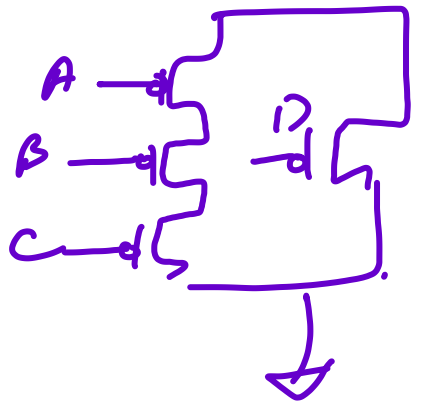
Cell width = 4 WT = 32 λ

∴ Area = 32 λ x 40 λ

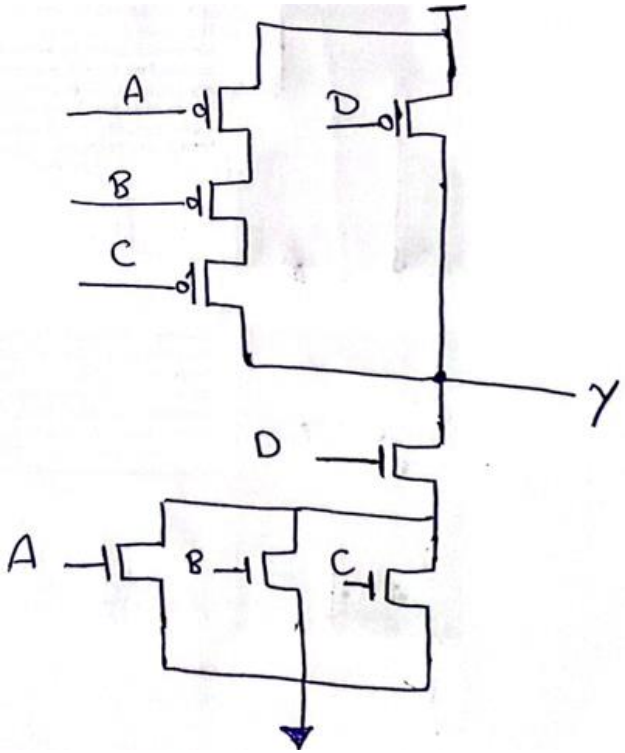
Example.11

Find the logic expression for the following gate & Draw CMOS circuit





- Solution:



$$Y = \overline{(A+B+C)\cdot D}$$

logic expression

OAI32

Example.12

Consider the design of a CMOS compound OR-AND-INVERT (OAI21) gate computing $F = \overline{(A + B).C}$

a) sketch a transistor-level schematic
b) sketch a stick diagram
c) estimate the area from the stick diagram

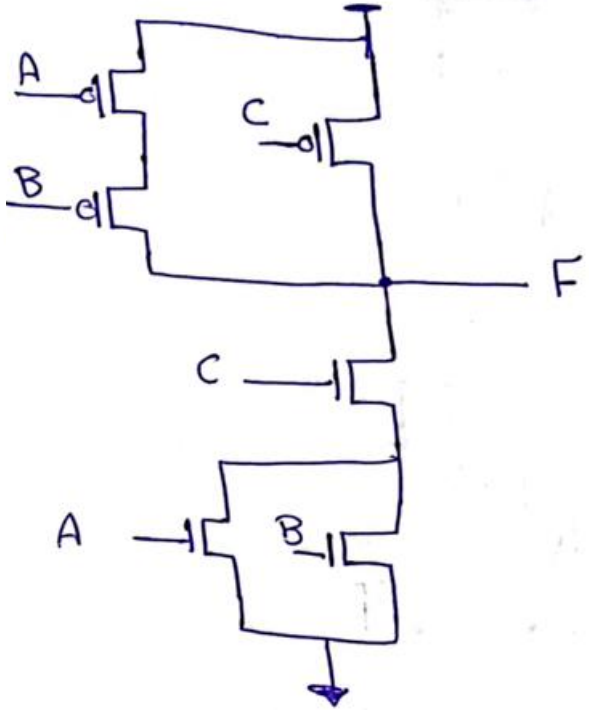
NOR

OI3

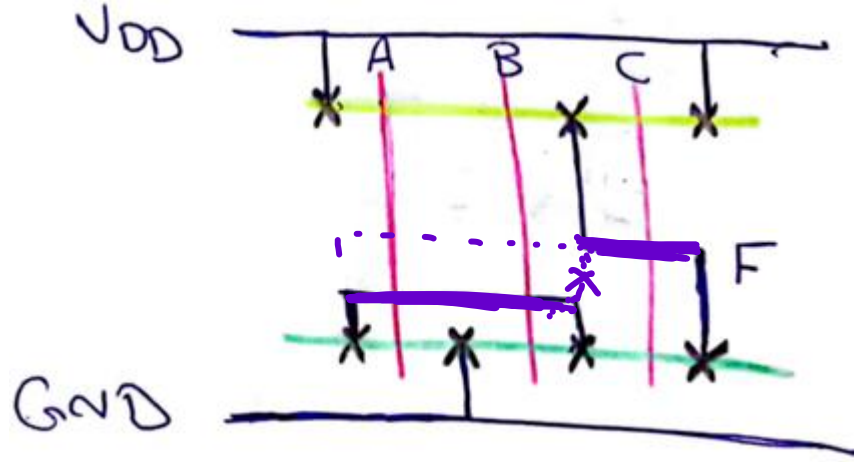
O3I

- Solution:

(a)



b)



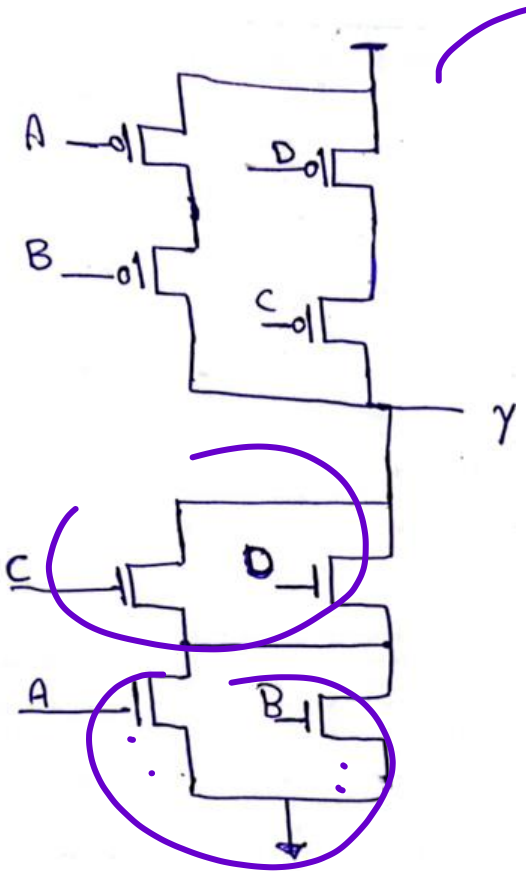
c)

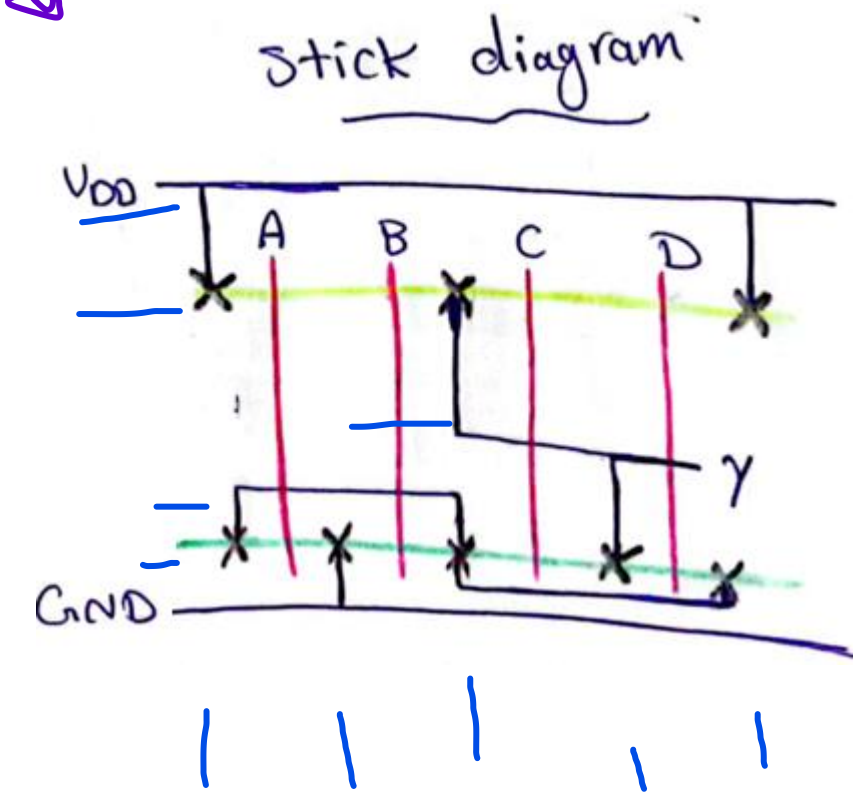
Cell area = 4WT x 6WT
= 32λ x 48λ

Example.13

Sketch a stick diagram for a CMOS gate computing $Y = \overline{(A + B).(C + D)}$ and estimate the cell width and height.

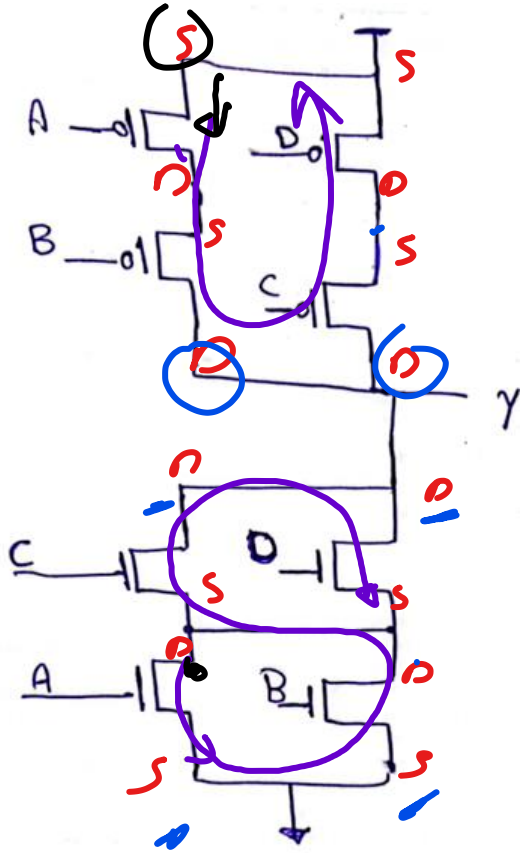
- Solution:

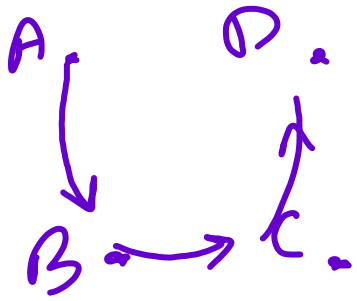


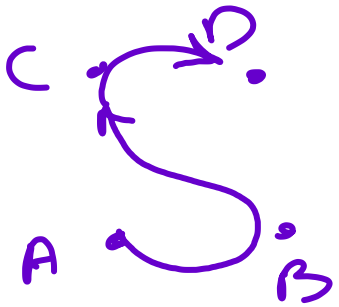


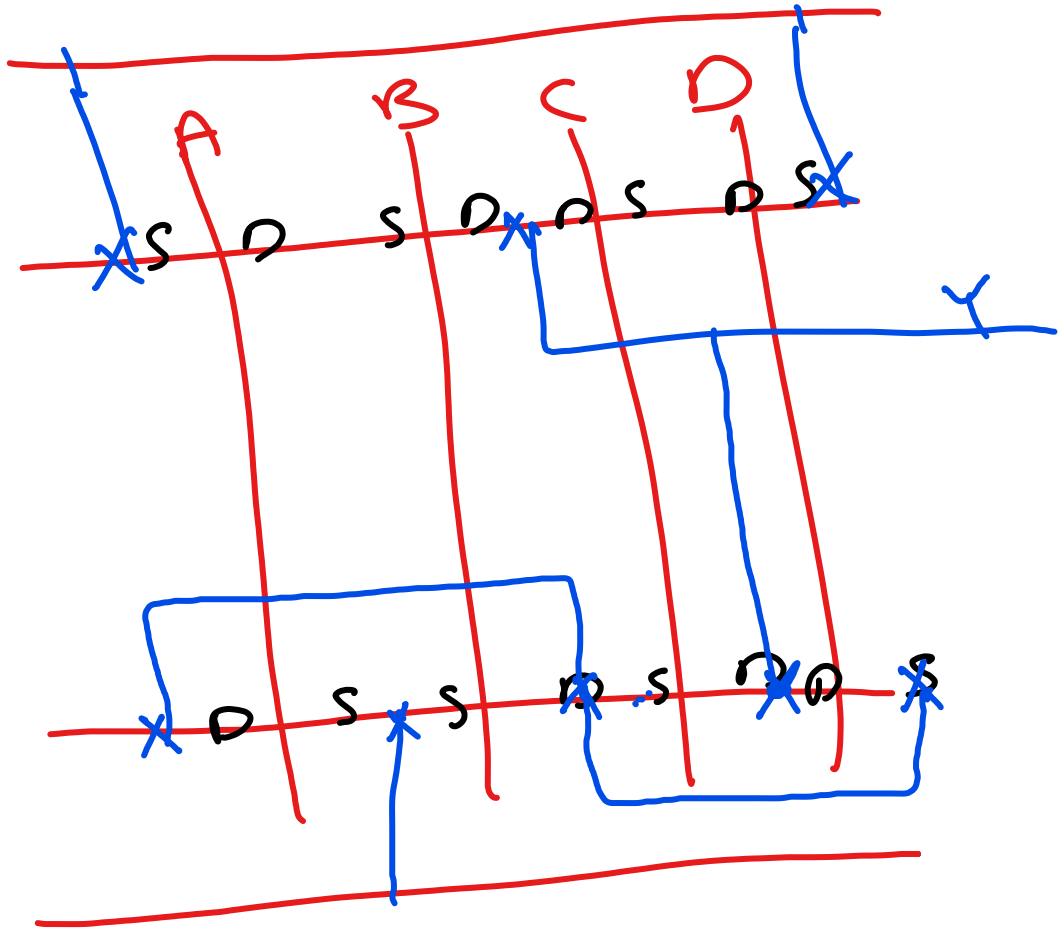
Cell width = 5WT = 40λ

Cell height = 7WT = 48λ


A
B
C
D
Y


A
B
C
D

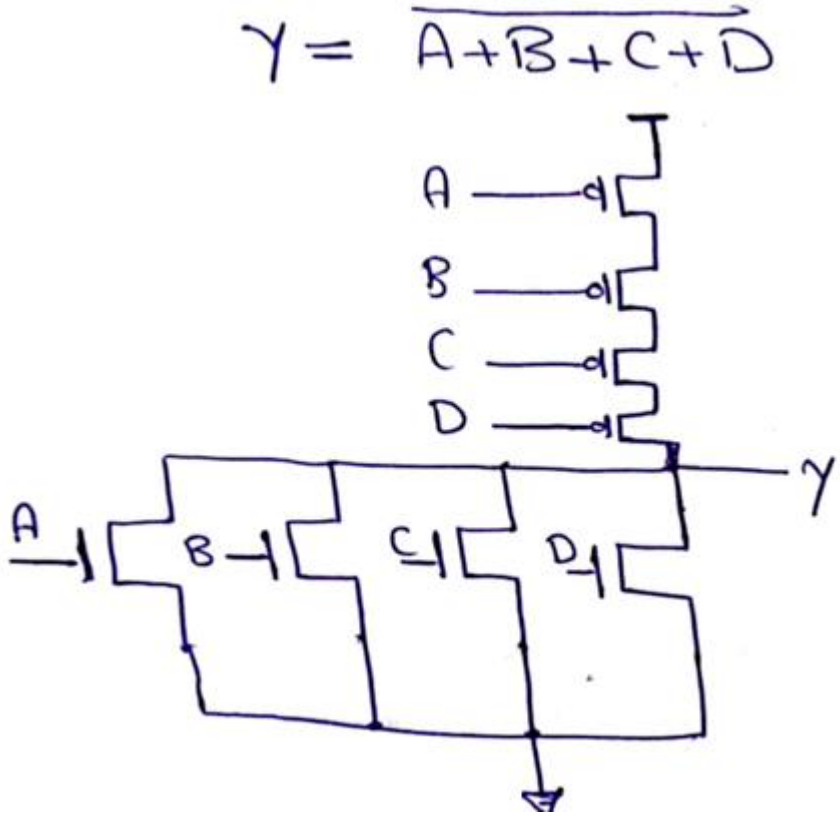

C
D
A
B

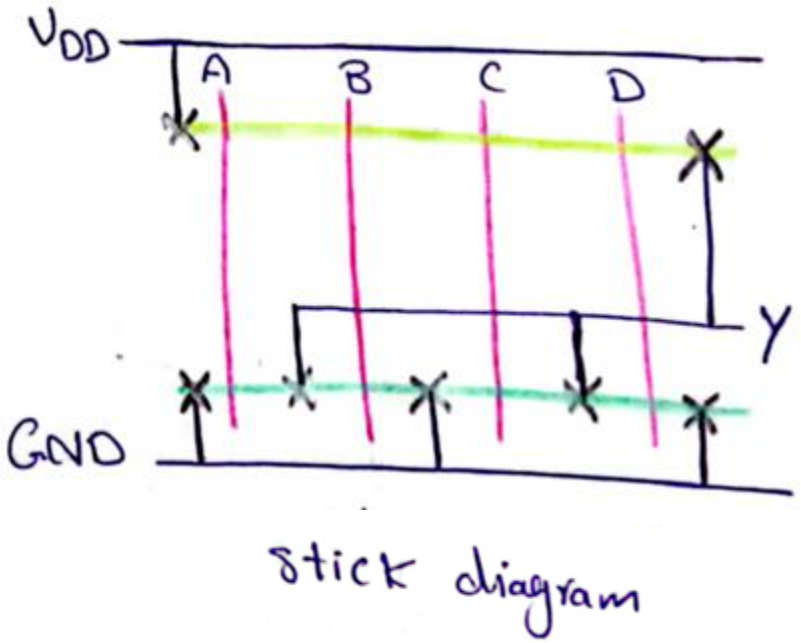

A
B
C
D
Y

Example.14

Sketch a stick diagram for a CMOS 4-input NOR gate and estimate the cell width and height.

- Solution:





Stick diagram

- Cell width = 5 WT
  = 40 λ
- Cell height = 5 WT
  = 40 λ

Example.15

Use combinations of a CMOS transistors to implement function $F = \overline{AB + C(D + E)}$

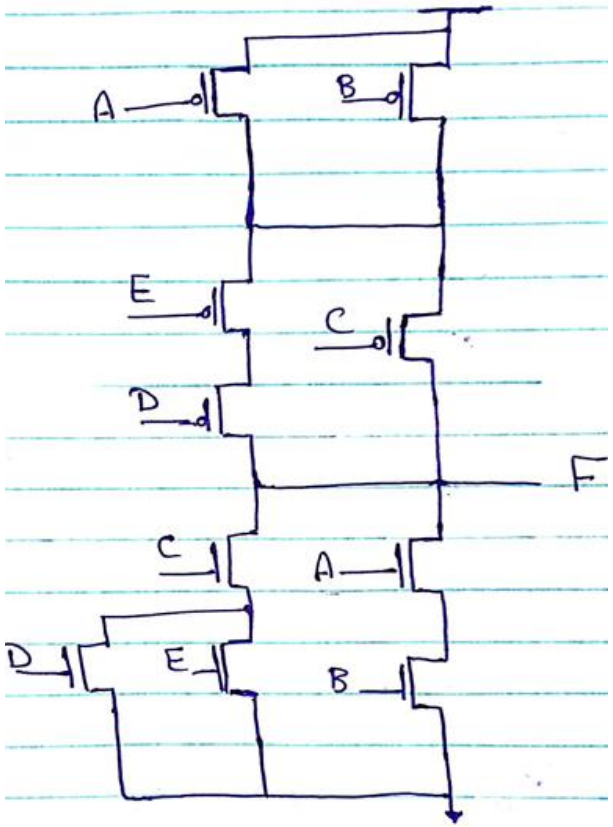
a) sketch a transistor-level schematic

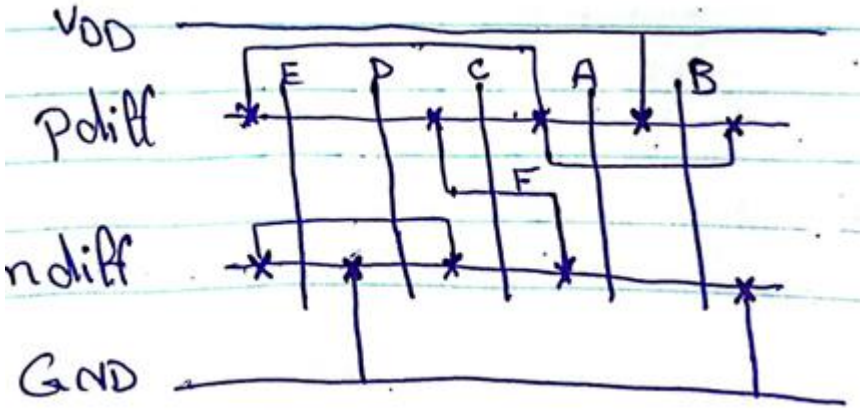
b) sketch a stick diagram for F

c) estimate the area from the stick diagram

d) layout your gate using unit-sized transistors.

- Solution:



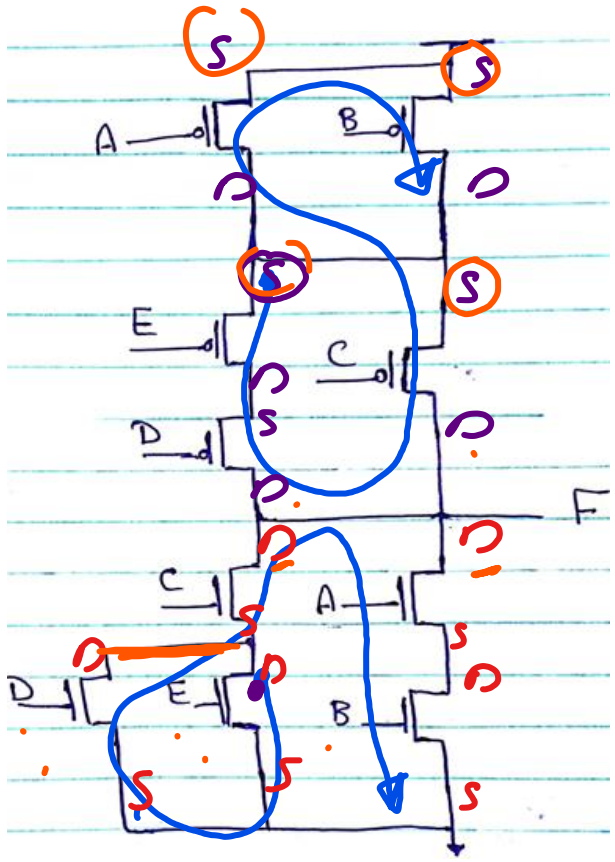


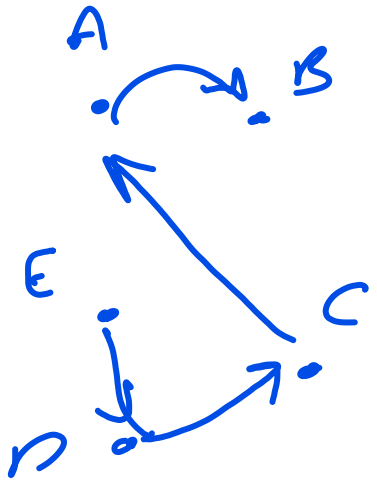
cell width = 6WT = 6x8λ = 48λ

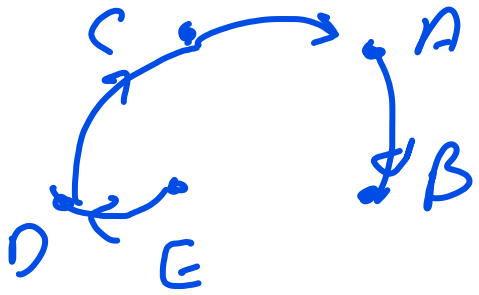
cell height = 8WT = 7x8λ = 56λ

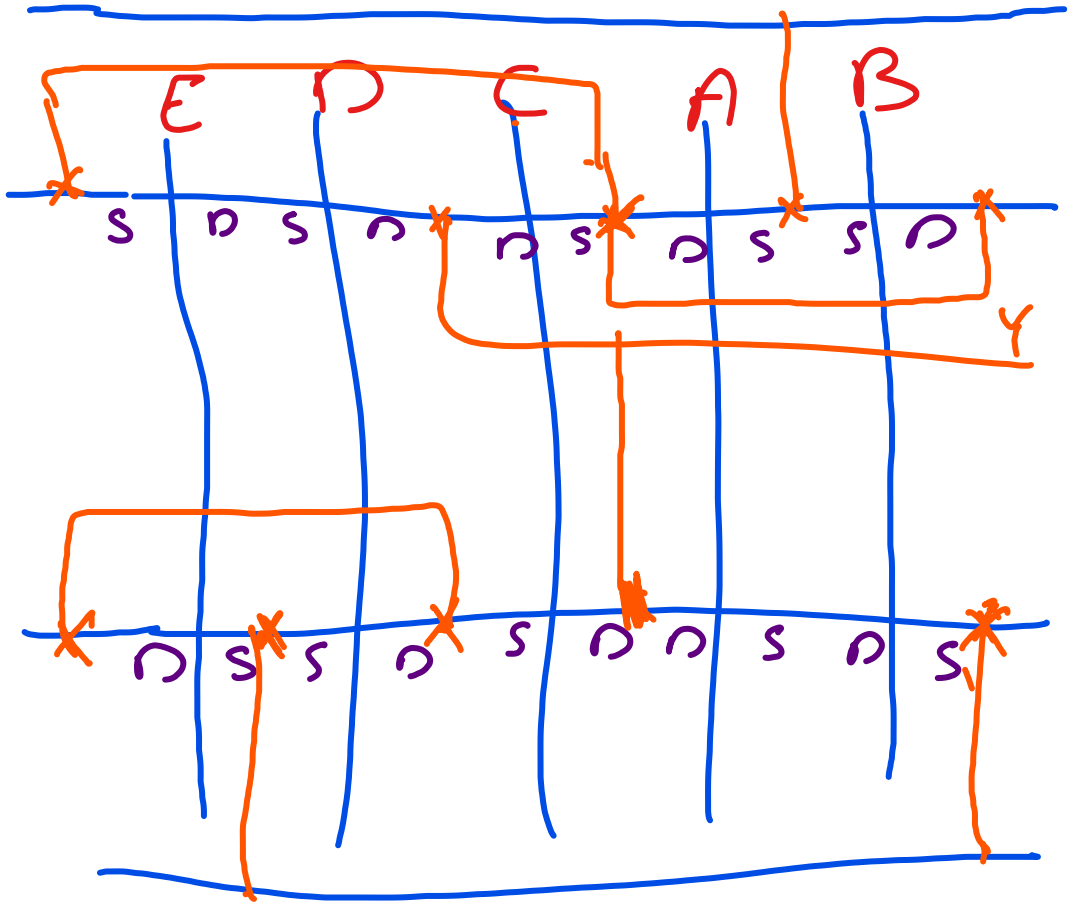
• Minimum area (without adding 4λ)

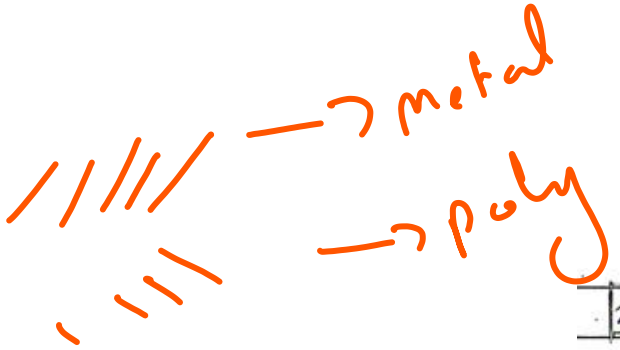
= 44λ x 52λ

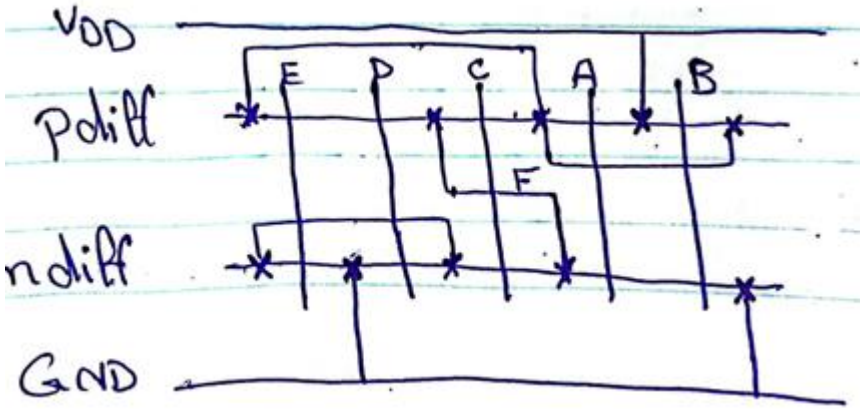

A
B
E
C
D
F

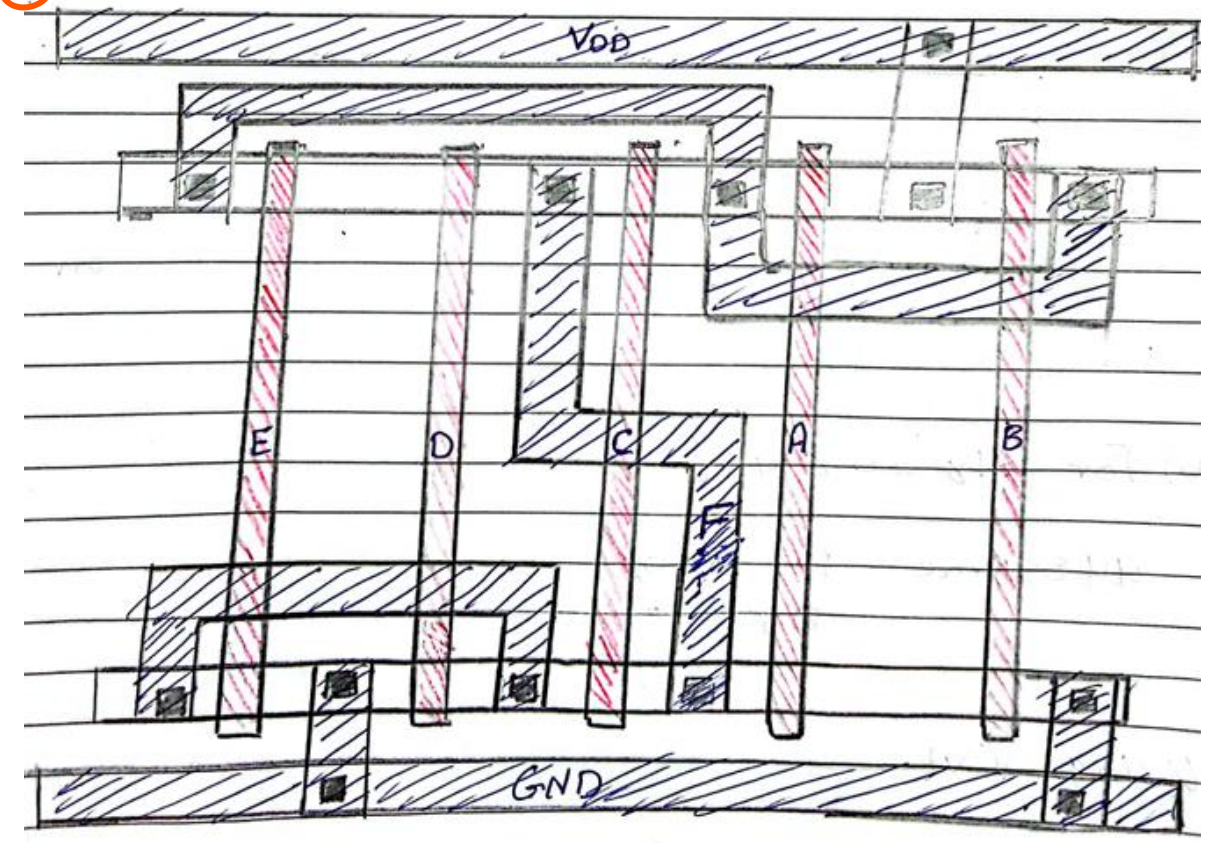

A
B
E
C
D


C
D
B
D
E


E
D
C
A
B
Y

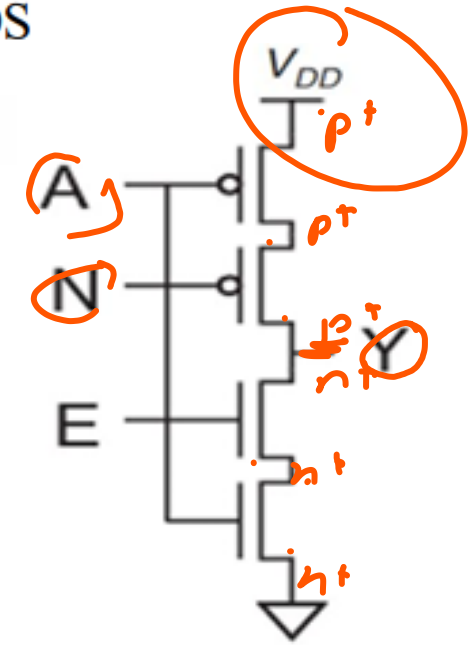

metal
poly


VDD
Pdiff
ndiff
GND
E
D
C
A
B
F

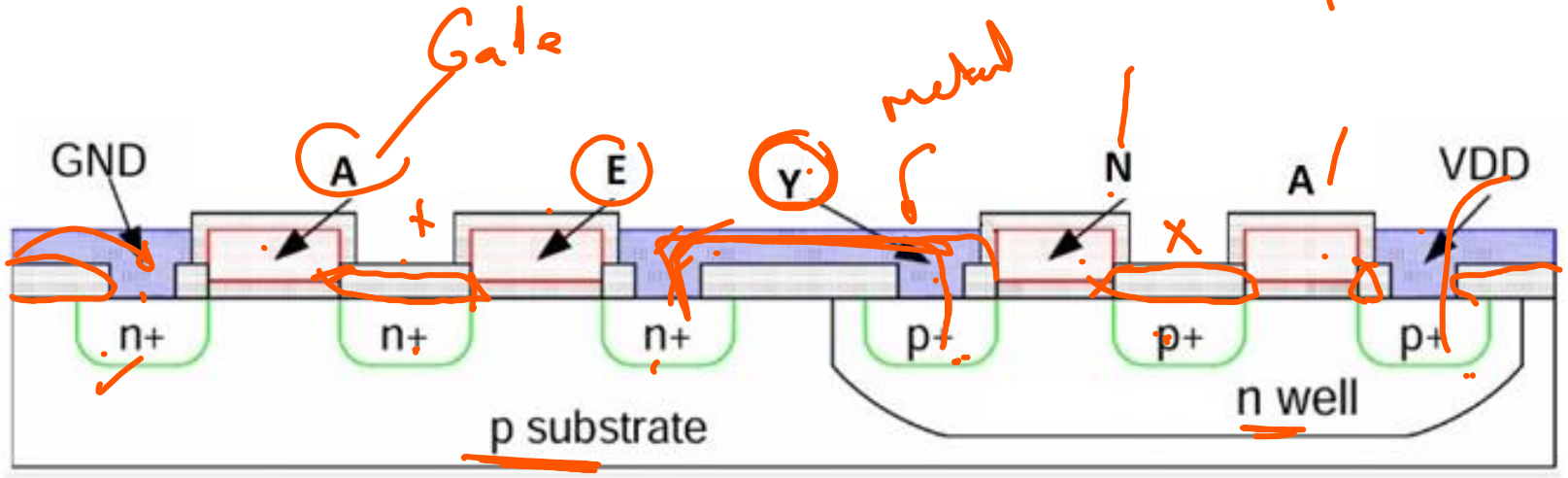

VDD
E
D
C
F
A
B
GND

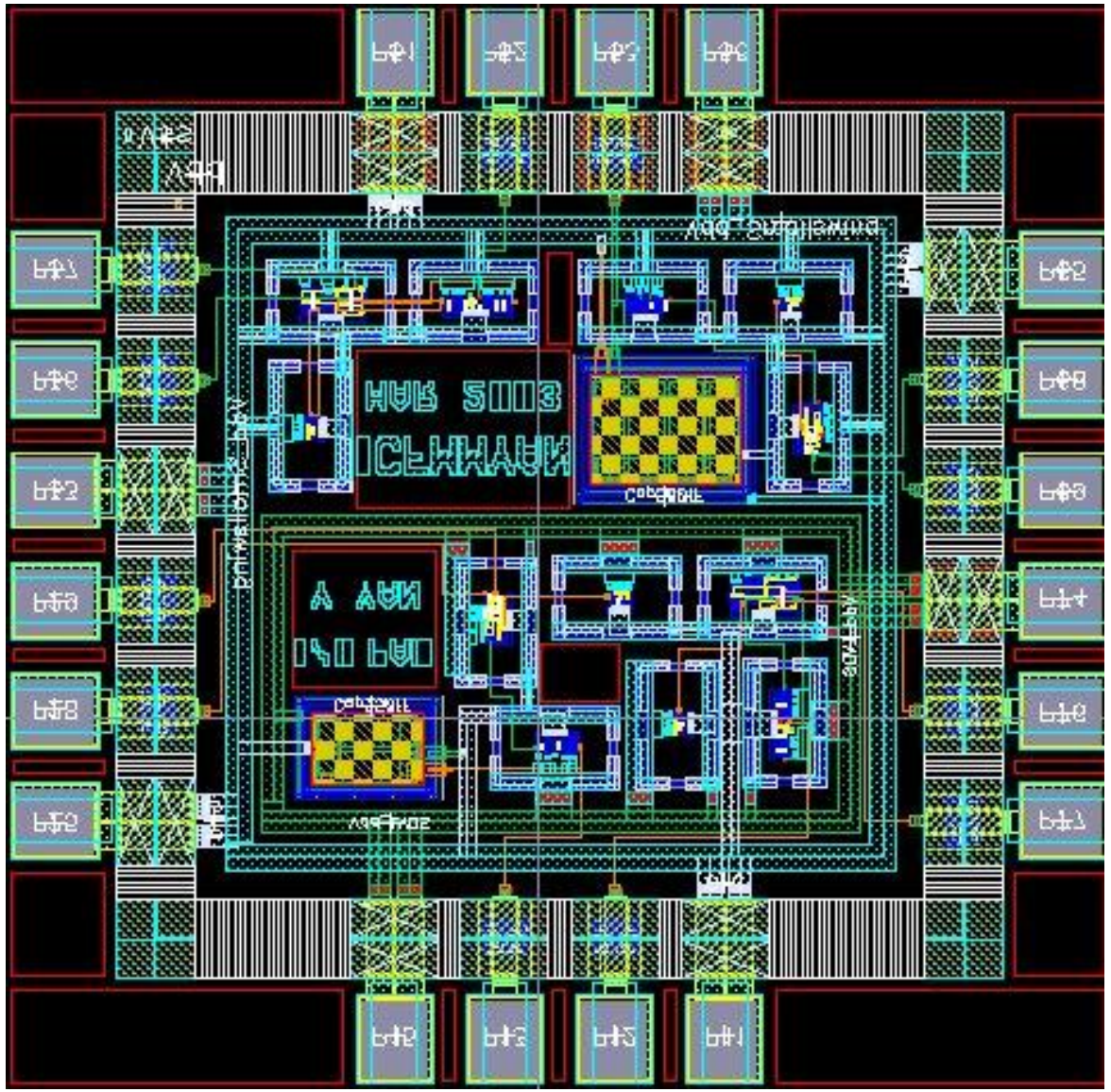
Example.16

Draw the cross section of the circuit shown below using n-well technology final cross-section should include the LOCOS isolation and metal terminals.



- Solution:





End of Lec.6

Any Questions